# Results of L22

	Document ID	Issue Date	Title	Current OR	Current XRef
1	US 5524007 A	19960604	Network interface architecture for a packet switch communication system	370/419	370/468
2	US 5517505 A		Synchronization method and apparatus for a wireless packet network	370/350	370/349; 370/508; 375/356; 375/366
3	US 5517500 A	19960514	Packet handling method	370/392	340/825.52
4	US 5495482 A	19960227	Packet transmission system and method utilizing both a data bus and dedicated control lines	370/419	370/473
5	US 5477541 A	1	Addressing technique for storing and referencing packet data		370/412; 370/428
6	US 5475681 A		Wireless in-building telecommunications system for voice and data communications	370/349	370/346; 370/347; 370/463; 370/473; 455/507

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	4386	(emulat\$5 and verif\$7) and (protocol and (logic or hardware or circuit or chip or ic))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR .	ON	2004/11/10 17:35
L2	1354	L1 and (packet and header)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/10 17:36
L3	157	L2 and vIsi	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/10 17:35
L4	26	(emulat\$5 and verif\$7) and (protocol same(logic or hardware or circuit or chip or ic) same visi)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/10 17:36
L5	17	L4 and (packet and header)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/10 17:36
L6	115	(emulat\$5 or verif\$7) and (protocol same (logic or hardware or circuit or chip or ic) same vlsi)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/10 17:38
L7	74	l6 and @ad<"20001020"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/10 18:30
L8	0	((emulat\$5 or verif\$7) and (protocol) and (logic or hardware or circuit or chip or ic) and vlsi).ab.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/10 17:39
L9	154	((emulat\$5 or verif\$7) and (protocol) and (logic or hardware or circuit or chip or ic or vlsi)).ab.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/10 17:40
L10	110	l9 and @ad<"20001020"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/10 17:40
L11	4	((emulat\$5 and verif\$7) and (protocol) and (logic or hardware or circuit or chip or ic or vlsi)).ab.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/10 17:40
L,12	2	l11 and @ad<"20001020"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/10 17:40

L13	4247	(incoming same packet same register) (command same decode same block)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/10 18:30
L14	10	(incoming same packet same register) and (outgoing same packet same register) and (command same decode same block)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/10 18:30
L15	8	I14 and @ad<"20001020"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/10 19:08
L16	7	I15 and (id or identification)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/10 19:08
L17	6	I15 and ((id or identification) same register)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/10 19:08
L18	6	I15 and ((id or identification) with register)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/10 19:08
L19	7	I15 and (address with register)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/10 19:09
L20	6	I18 and (address with register)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/10 19:25
L21	1191934	I20 and memory mode	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/10 19:25
L22	6	I20 and (memory same mode)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/10 19:26
S1	1	"5546562".pn.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/10 18:29
S2	53	"5546562".uref.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/08 20:20

<b>S</b> 3	2048	packet same protocol same logic	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/08 20:21
S4	2743	size same request same packets	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/08 20:25
S5	262	S3 and S4	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/08 20:22
· S6	167	S5 and ((id or identification) same field)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/08 20:23
S7	159	S6 and (address same bits)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/08 20:24
S8	88	S7 and ((data with bits) same register)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/08 20:25
S9	102	S7 and ((data with bits) same (memory or memories))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/08 20:25
S10	159	S6 and (address same bit)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/08 20:24
S11	88	S7 and ((data with bit) same register)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/08 20:25
S12	65	S8 and ((data with bit) same (memory or memories))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/08 20:25
S13	60	S12 and (size same (request with packets))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/08 20:26
S14	13	S13 and (tag same field) and (command same field) and (data same field)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/08 20:29

S15	9	S14 and (verify or verification)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/08 20:35
S16	13	S14 and (packet same register)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/08 20:35
S17	9	S15 and (packet same register)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/08 20:36
S18	9	S17 and (buffer)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/08 20:36
S19	9	S17 and (data same buffer)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/08 20:43
S20	1	S17 and ((input or output) same (data same buffer))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/08 20:37
S21	1019	design same under same (verify or verification)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/08 20:43
S22	7	S21 and duv	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/08 20:43
S23	204	(simulat\$5 or emulat\$5) and (x adj "25")	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/10 15:45
S24	26	S23 and (packet and header)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/10 15:47
S26	24	S24 and (hardware)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/10 10:41
S27	2215	(emulat\$5 and verif\$7) and (protocol same (logic or hardware or circuit or chip or ic))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/10 15:52

S28	818	S27 and (packet and header)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/10 15:53
S29	121	S28 and vlsi	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/10 15:53
S30	74	S29 and (packet same header)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/10 15:50
S31	74	S30 and ((protocol same (logic or hardware or circuit or chip or ic)))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/10 15:51
S32	17	S31 and (protocol same vlsi)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/10 15:51
S33	4386	(emulat\$5 and verif\$7) and (protocol and (logic or hardware or circuit or chip or ic))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/10 15:52
S35	1354	S33 and (packet and header)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/10 15:53

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January 1980 ACM SIGACT News, Volume 12 Issue 1

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The Parallel Protocol Engine

Matthias Kaiserswerth

December 1993 IEEE/ACM Transactions on Networking (TON), Volume 1 Issue 6

Full text available: pdf(1.65 MB)

Additional Information: full citation, references, citings, index terms, review

3 A low power, low bandwidth protocol for remote wireless terminals George Hadjiyiannis, Anantha Chandrakasan, Srinivas Devadas

January 1998 Wireless Networks, Volume 4 Issue 1

Full text available: pdf(474.12 KB) Additional Information: full citation, abstract, references, index terms

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4 Xunet 2: lessons from an early wide-area ATM testbed

Charles R. Kalmanek, Srinivasan Keshav, William T. Marshall, Samuel P. Morgan, Robert C. Restrick

February 1997 IEEE/ACM Transactions on Networking (TON), Volume 5 Issue 1

Full text available: pdf(231.69 KB) Additional Information: full citation, references, index terms

Keywords: asynchronous transfer mode, available bit rate, constant bit rate, variable bit rate

5 <u>A pipelined, multiprocessor architecture for a connectionless server for broadband ISDN</u>

Daniel S. Omundsen, A. Roger Kaye, Samy A. Mahmoud April 1994 IEEE/ACM Transactions on Networking (TON), Volume 2 Issue 2

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The transport layer: tutorial and survey
Sami Iren, Paul D. Amer, Phillip T. Conrad
December 1999 ACM Computing Surveys (CSUR), Volume 31 Issue 4

Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index</u>

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A parallel embedded-processor architecture for ATM reassembly Richard F. Hobson, P. S. Wong

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8 Reliable broadcast algorithms for HARTS

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November 1991 ACM Transactions on Computer Systems (TOCS), Volume 9 Issue 4

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9 Wormhole IP over (connectionless) ATM

Manolis G. H. Katevenis, Iakovos Mavroidis, Georgios Sapountzis, Eva Kalyvianaki, Ioannis Mavroidis, Georgios Glykopoulos

October 2001 IEEE/ACM Transactions on Networking (TON), Volume 9 Issue 5

Full text available: pdf(211.25 KB)

Additional Information: full citation, abstract, references, citings, index terms

High-speed switches and routers internally operate using fixed-size cells or segments; variable-size packets are segmented and later reassembled. Connectionless ATM was proposed to quickly carry IP packets segmented into cells (AAL5) using a number of hardware-managed ATM VCs. We show that this is analogous to wormhole routing. We modify this architecture to make it applicable to existing ATM equipment: we propose a low-

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Keywords: Connectionless ATM, IP over ATM, gigabit router, routing filter, wormhole IP, wormhole routing

<sup>10</sup> A reconfigurable hardware approach to network simulation

Dimitrios Stiliadis, Anujan Varma

January 1997 ACM Transactions on Modeling and Computer Simulation (TOMACS), Volume 7 Issue 1

Full text available: pdf(925.18 KB) Additional Information: full citation, references, citings, index terms, review

**Keywords**: ATM switch scheduling, field-programmable gate array, hardware simulation

11 Architectural exploration and system simulations: A modular simulation framework for architectural exploration of on-chip interconnection networks

Tim Kogel, Malte Doerper, Andreas Wieferink, Rainer Leupers, Gerd Ascheid, Heinrich Meyr, Serge Goossens

October 2003 Proceedings of the 1st IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis

Full text available: pdf(163.88 KB)

Additional Information: full citation, abstract, references, citings, index terms

Ever increasing complexity and heterogeneity of SoC platforms require diversified on-chip communication schemes beyond the currently omnipresent shared bus architectures. To prevent time consuming design changes late in the design flow, we propose the early exploration of the on-chip communication architecture to meet performance and cost requirements. Based on SystemC 2.0.1 we have defined a modular exploration framework, which is able to capture the effect on performance for different on-chip ...

**Keywords**: SystemC, architecture exploration, network-on-chip, simulation

12 Distributed operating systems

Andrew S. Tanenbaum, Robbert Van Renesse

December 1985 ACM Computing Surveys (CSUR), Volume 17 Issue 4

Full text available: pdf(5.49 MB)

Additional Information: full citation, abstract, references, citings, index terms, review

Distributed operating systems have many aspects in common with centralized ones, but they also differ in certain ways. This paper is intended as an introduction to distributed operating systems, and especially to current university research about them. After a discussion of what constitutes a distributed operating system and how it is distinguished from a computer network, various key design issues are discussed. Then several examples of current research projects are examined in some detail ...

13 An Ethernet compatible low cost/high performance communication solution

I. Chlamtac, A. Herman

August 1987 ACM SIGCOMM Computer Communication Review, Proceedings of the ACM workshop on Frontiers in computer communications technology, Volume 17 Issue 5

Additional Information: full citation, abstract, references, index terms Full text available: pdf(1.24 MB)

The LAN-HUB is a new local area network designed to combine the properties of several

existing LAN standards to provide highly reliable communication at a relatively lower cost per station, improve network capacity/delay performance and increase the LAN user's flexibility in configuring his network. The LAN-HUB network is configured around the CODEX 4320 LAN-HUB communication controllers which allow up to eight Ethernet/IEEE 802.3 stations to transparently share one network transceiver or R ...

14 Energy Awareness and Power Control: Topology management for sensor networks: exploiting latency and density



Curt Schurgers, Vlasios Tsiatsis, Saurabh Ganeriwal, Mani Srivastava June 2002 Proceedings of the 3rd ACM international symposium on Mobile ad hoc networking & computing

Full text available: pdf(597.09 KB)

Additional Information: full citation, abstract, references, citings, index terms

In wireless sensor networks, energy efficiency is crucial to achieve satisfactory network lifetime. In order to reduce the energy consumption of a node significantly, its radio needs to be turned off. Yet, some nodes have to participate in multi-hop packet forwarding. We tackle this issue by exploiting two degrees of freedom in topology management: the path setup latency and the network density. First, we propose a new technique called Sparse Topology and Energy Management (STEM), which aggressi ...

**Keywords**: sensor networks, shutdown, topology management, wakeup

<sup>15</sup> ROMM routing on mesh and torus networks

Ted Nesson, S. Lennart Johnsson

July 1995 Proceedings of the seventh annual ACM symposium on Parallel algorithms and architectures

Full text available: pdf(1.37 MB)

Additional Information: full citation, references, citings, index terms

16 Design, implementation, and performance measurement of a native-mode ATM transport layer (extended version)

R. Ahuja, S. Keshav, H. Saran

August 1996 IEEE/ACM Transactions on Networking (TON), Volume 4 Issue 4

Full text available: pdf(1.66 MB)

Additional Information: full citation, references, index terms

**Keywords**: AAL 5, asynchronous transfer mode, native-mode ATM, personal computer, transport layer

17 A structural view of the Cedar programming environment

Daniel C. Swinehart, Polle T. Zellweger, Richard J. Beach, Robert B. Hagmann August 1986 ACM Transactions on Programming Languages and Systems (TOPLAS), Volume 8 Issue 4

Full text available: pdf(6.32 MB)

Additional Information: full citation, abstract, references, citings, index terms

This paper presents an overview of the Cedar programming environment, focusing on its overall structure—that is, the major components of Cedar and the way they are organized. Cedar supports the development of programs written in a single programming language, also called Cedar. Its primary purpose is to increase the productivity of programmers whose activities include experimental programming and the development of prototype software systems for a high-performance personal computer. T ...

18 Improving parallel system performance by changing the arrangement of the network links



V. Puente, C. Izu, J. A. Gregorio, R. Beivide, J. M. Prellezo, F. Vallejo May 2000 Proceedings of the 14th international conference on Supercomputing

Full text available: pdf(922.78 KB) Additional Information: full citation, abstract, references, index terms

The Midimew network is an excellent contender for implementing the communication subsystem of a high performance computer. This network is an optimal 2D topology in the sense there are no other symmetric direct networks of degree 4 with a lower average distance or diameter. In fact, it reduces the diameter of the well known torus network by approximately □ 2. Although the topology was proposed and analyzed a decade ago, the lack of simple deadlock avoidance mechanisms prevented its ut ...

19 High performance communications in processor networks

C. R. Jesshope, P. R. Miller, J. T. Yantchev

April 1989 ACM SIGARCH Computer Architecture News, Proceedings of the 16th annual international symposium on Computer architecture, Volume 17 Issue 3

Full text available: pdf(1.11 MB)

Additional Information: full citation, abstract, references, citings, index

In order to provide an arbitrary and fully dynamic connectivity in a network of processors, transport mechanisms must be implemented, which provide the propagation of data from processor to processor, based on addresses contained within a packet of data. Such data transport mechanisms must satisfy a number of requirements - deadlock and livelock freedom, good hot-spot performance, high throughput and low latency. This paper proposes a solution to these problems, which allows deadlock free, ...

<sup>20</sup> A decade of reconfigurable computing: a visionary retrospective

March 2001 Proceedings of the conference on Design, automation and test in Europe

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January 1980 ACM SIGACT News, Volume 12 Issue 1

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<sup>2</sup> The Parallel Protocol Engine

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Daniel S. Omundsen, A. Roger Kaye, Samy A. Mahmoud April 1994 IEEE/ACM Transactions on Networking (TON), Volume 2 Issue 2

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The transport layer: tutorial and survey Sami Iren, Paul D. Amer, Phillip T. Conrad December 1999 ACM Computing Surveys (CSUR), Volume 31 Issue 4

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Reliable broadcast algorithms for HARTS

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November 1991 ACM Transactions on Computer Systems (TOCS), Volume 9 Issue 4

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Full text available: pdf(163.88 KB)

Additional Information: full citation, abstract, references, citings, index terms

Ever increasing complexity and heterogeneity of SoC platforms require diversified on-chip communication schemes beyond the currently omnipresent shared bus architectures. To prevent time consuming design changes late in the design flow, we propose the early exploration of the on-chip communication architecture to meet performance and cost requirements. Based on SystemC 2.0.1 we have defined a modular exploration framework, which is able to capture the effect on performance for different on-chip ...

**Keywords**: SystemC, architecture exploration, network-on-chip, simulation

12 Distributed operating systems

Andrew S. Tanenbaum, Robbert Van Renesse December 1985 ACM Computing Surveys (CSUR), Volume 17 Issue 4

Full text available: pdf(5.49 MB)

Additional Information: full citation, abstract, references, citings, index terms, review

Distributed operating systems have many aspects in common with centralized ones, but they also differ in certain ways. This paper is intended as an introduction to distributed operating systems, and especially to current university research about them. After a discussion of what constitutes a distributed operating system and how it is distinguished from a computer network, various key design issues are discussed. Then several examples of current research projects are examined in some detail ...

<sup>13</sup> An Ethernet compatible low cost/high performance communication solution

I. Chlamtac, A. Herman

August 1987 ACM SIGCOMM Computer Communication Review , Proceedings of the ACM workshop on Frontiers in computer communications technology, Volume 17 Issue 5

Full text available: pdf(1.24 MB) Additional Information: full citation, abstract, references, index terms

The LAN-HUB is a new local area network designed to combine the properties of several

existing LAN standards to provide highly reliable communication at a relatively lower cost per station, improve network capacity/delay performance and increase the LAN user's flexibility in configuring his network. The LAN-HUB network is configured around the CODEX 4320 LAN-HUB communication controllers which allow up to eight Ethernet/IEEE 802.3 stations to transparently share one network transceiver or R ...

14 Energy Awareness and Power Control: Topology management for sensor networks: exploiting latency and density



Curt Schurgers, Vlasios Tsiatsis, Saurabh Ganeriwal, Mani Srivastava

June 2002 Proceedings of the 3rd ACM international symposium on Mobile ad hoc networking & computing

Full text available: T pdf(597.09 KB)

Additional Information: full citation, abstract, references, citings, index terms

In wireless sensor networks, energy efficiency is crucial to achieve satisfactory network lifetime. In order to reduce the energy consumption of a node significantly, its radio needs to be turned off. Yet, some nodes have to participate in multi-hop packet forwarding. We tackle this issue by exploiting two degrees of freedom in topology management: the path setup latency and the network density. First, we propose a new technique called Sparse Topology and Energy Management (STEM), which aggressi ...

**Keywords**: sensor networks, shutdown, topology management, wakeup

15 ROMM routing on mesh and torus networks

Ted Nesson, S. Lennart Johnsson

July 1995 Proceedings of the seventh annual ACM symposium on Parallel algorithms and architectures

Full text available: pdf(1.37 MB)

Additional Information: full citation, references, citings, index terms

16 Design, implementation, and performance measurement of a native-mode ATM transport layer (extended version)

R. Ahuja, S. Keshav, H. Saran

August 1996 IEEE/ACM Transactions on Networking (TON), Volume 4 Issue 4

Full text available: pdf(1.66 MB)

Additional Information: full citation, references, index terms

Keywords: AAL 5, asynchronous transfer mode, native-mode ATM, personal computer, transport layer

17 A structural view of the Cedar programming environment

Daniel C. Swinehart, Polle T. Zellweger, Richard J. Beach, Robert B. Hagmann August 1986 ACM Transactions on Programming Languages and Systems (TOPLAS), Volume 8 Issue 4

Full text available: pdf(6.32 MB)

Additional Information: full citation, abstract, references, citings, index terms

This paper presents an overview of the Cedar programming environment, focusing on its overall structure—that is, the major components of Cedar and the way they are organized. Cedar supports the development of programs written in a single programming language, also called Cedar. Its primary purpose is to increase the productivity of programmers whose activities include experimental programming and the development of prototype software systems for a high-performance personal computer. T ...

18 Improving parallel system performance by changing the arrangement of the network links



V. Puente, C. Izu, J. A. Gregorio, R. Beivide, J. M. Prellezo, F. Vallejo May 2000 Proceedings of the 14th international conference on Supercomputing

Full text available: 📆 pdf(922.78 KB). Additional Information: full citation, abstract, references, index terms

The Midimew network is an excellent contender for implementing the communication subsystem of a high performance computer. This network is an optimal 2D topology in the sense there are no other symmetric direct networks of degree 4 with a lower average distance or diameter. In fact, it reduces the diameter of the well known torus network by approximately □ 2. Although the topology was proposed and analyzed a decade ago, the lack of simple deadlock avoidance mechanisms prevented its ut ...

19 High performance communications in processor networks

C. R. Jesshope, P. R. Miller, J. T. Yantchev

April 1989 ACM SIGARCH Computer Architecture News, Proceedings of the 16th annual international symposium on Computer architecture, Volume 17 Issue 3

Full text available: pdf(1.11 MB)

Additional Information: full citation, abstract, references, citings, index terms

In order to provide an arbitrary and fully dynamic connectivity in a network of processors, transport mechanisms must be implemented, which provide the propagation of data from processor to processor, based on addresses contained within a packet of data. Such data transport mechanisms must satisfy a number of requirements - deadlock and livelock freedom, good hot-spot performance, high throughput and low latency. This paper proposes a solution to these problems, which allows deadlock free, ...

<sup>20</sup> A decade of reconfigurable computing: a visionary retrospective

R. Hartenstein

March 2001 Proceedings of the conference on Design, automation and test in Europe

Full text available: pdf(768.00 KB) Additional Information: full citation, references, citings, index terms

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1 On contention resolution protocols and associated probabilistic phenomena P. D. MacKenzie, C. G. Plaxton, R. Rajaraman

March 1998 Journal of the ACM (JACM), Volume 45 Issue 2

Full text available: pdf(389.75 KB)

Additional Information: full citation, abstract, references, citings, index terms, review

Consider an on-line scheduling problem in which a set of abstract processes are competing for the use of a number of resources. Further assume that it is either prohibitively expensive or impossible for any two of the processes to directly communicate with one another. If several processes simultaneously attempt to allocate a particular resource (as may be expected to occur, since the processes cannot easily coordinate their allocations), then none succeed. In such a framework, it is a chal ...

**Keywords**: emulation protocols, hash functions, parallel computation

2 A parallel embedded-processor architecture for ATM reassembly

Richard F. Hobson, P. S. Wong

February 1999 IEEE/ACM Transactions on Networking (TON), Volume 7 Issue 1

Full text available: pdf(331.21 KB) Additional Information: full citation, references, citings, index terms

Keywords: ATM, embedded systems, medium access control, segmentation and reassembly

<sup>3</sup> A generic architecture for on-chip packet-switched interconnections

Pierre Guerrier, Alain Greiner

January 2000 Proceedings of the conference on Design, automation and test in Europe

Full text available: pdf(100.74 KB)

Publisher Site

Additional Information: full citation, references, citings, index terms

A low power, low bandwidth protocol for remote wireless terminals George Hadjiyiannis, Anantha Chandrakasan, Srinivas Devadas

January 1998 Wireless Networks, Volume 4 Issue 1

Full text available: pdf(474.12 KB) Additional Information: full citation, abstract, references, index terms

We present a low bandwidth protocol for wireless multi-media terminals targeted towards low power consumption on the terminal side. With the widespread use of portable computing devices, low power has become a major design criterion. One way of minimizing power consumption is to perform all tasks, other than managing hardware for the display and input, on a stationary workstation and exchange information between that workstation and the portable terminal via a wireless link. A protocol for ...

#### 5 LimitLESS directories: A scalable cache coherence scheme

David Chaiken, John Kubiatowicz, Anant Agarwal

April 1991 Proceedings of the fourth international conference on Architectural support for programming languages and operating systems, Volume 26, 19, 25 Issue 4, 2, Special Issue

Full text available: pdf(1.20 MB) Additional Information: full citation, references, citings, index terms

#### The Parallel Protocol Engine

Matthias Kaiserswerth

December 1993 IEEE/ACM Transactions on Networking (TON), Volume 1 Issue 6

Full text available: pdf(1.65 MB) Additional Information: full citation, references, citings, index terms, review

#### 7 A control and management network for wireless ATM systems

Stephen F. Bush, Sunil Jagannath, Ricardo Sanchez, Joseph B. Evans, Gary J. Minden, K. Sam Shanmugan, Victor S. Frost

September 1997 Wireless Networks, Volume 3 Issue 4

Additional Information: full citation, abstract, references, citings, index Full text available: pdf(573.05 KB) terms

This paper describes the design of a control and management network (orderwire) for a mobile wireless Asynchronous Transfer Mode (ATM) network. This mobile wireless ATM network is part of the Rapidly Deployable Radio Network (RDRN). The orderwire system consists of a packet radio network which overlays the mobile wireless ATM network. Each network element in this network uses Global Positioning System (GPS) information to control a beamforming antenna subsystem which provides for spatial re ...

#### 8 Current issues in packet switch design

Cyriel Minkenberg, Ronald P. Luijten, François Abel, Wolfgang Denzel, Mitchell Gusat January 2003 ACM SIGCOMM Computer Communication Review, Volume 33 Issue 1

Full text available: 🔂 pdf(304.83 KB) Additional Information: full citation, abstract, references, index terms

Addressing the ever growing capacity demand for packet switches, current research focuses on scheduling algorithms or buffer bandwidth reductions. Although these topics remain relevant, our position is that the primary design focus for systems beyond 1 Tb/s must be shifted to aspects resulting from packaging disruptions. Based on trends such as increased link rates and improved CMOS technologies, we derive new design factors for such switch fabrics. For instance, we argue that the packet round-t ...

9 On contention resolution protocols and associated probabilistic phenomena P. D. MacKenzie, C. G. Plaxton, R. Rajaraman

May 1994 Proceedings of the twenty-sixth annual ACM symposium on Theory of computing

Full text available: pdf(1.09 MB) Additional Information: full citation, references, citings, index terms 10 Circuit emulation services over ethernet-part 2: prototype and experimental results James Aweya, Michel Ouellette, Delfin Y. Montuno, Jeganathan Markandu, Karin Sundstrom, Kent Felske January 2004 International Journal of Network Management, Volume 14 Issue 1 Full text available: Topdf(300.81 KB) Additional Information: full citation, abstract, references, index terms This paper describes a prototype implementation and experimental results for unstructured circuit emulation service (UCES) of T3 data stream over Ethernet. As explained in Part 1 of this paper, packet-switched networks such as Ethernet are not designed to transport TDM data and so have no inherent clock distribution and synchronization mechanisms. Thus, to allow the frequency of the source TDM stream to be regenerated at the receiver, the prototype employed the clock synchronization scheme descr ... <sup>11</sup> Methods for message routing in parallel machines Tom Leighton July 1992 Proceedings of the twenty-fourth annual ACM symposium on Theory of computing Full text available: Topdf(2.32 MB)

Additional Information: full citation, references, citings, index terms 12 Circuit emulation services over ethernet-part 1: clock synchronization using timestamps James Aweya, Michel Ouellette, Delfin Y. Montuno, Kent Felske January 2004 International Journal of Network Management, Volume 14 Issue 1 Full text available: Topdf(260.66 KB) Additional Information: full citation, abstract, references, index terms Due to Ethernet's ubiquity, simplicity, scalability and cost effectiveness there is significant customer demand for Ethernet-based access and transport in the metropolitan network. Many service providers have recognized this need and are currently establishing Ethernetbased services to meet this demand. The migration to all-Ethernet access will not be instantaneous since many customers currently have legacy TDM access interfaces on their routers and PBX equipment. Circuit Emulation Services (CE ... 13 Simulation and experiments: Detailed models for sensor network simulations and their impact on network performance Maneesh Varshney, Rajive Bagrodia October 2004 Proceedings of the 7th ACM international symposium on Modeling, analysis and simulation of wireless and mobile systems Full text available: Topdf(400.40 KB) Additional Information: full citation, abstract, references, index terms Recent trends in sensor network simulation can be divided between less flexible but accurate emulation based approach and more generic but less detailed network simulator models. We offer an approach with the flexibility of network simulators and provides the accuracy comparable to emulation based approaches. We describe the design and architecture of sensor network simulator which provides a rich suite of following models: sensing stack to model wave and diffusion based sensor channels, an accu ...

**Keywords**: sensor network, simulation

Verification (co-organized with LA-TTTC): A multi-level approach to the dependability

#### analysis of networked systems based on the CAN protocol

F. Corno, J. Pérez Acle, M. Sonza Reorda, M. Violante

September 2004 Proceedings of the 17th symposium on Integrated circuits and system design

Full text available: pdf(73.05 KB) Additional Information: full citation, abstract, references, index terms

Safety-critical applications are now common where both digital and mechanical components are deployed, as in the automotive fields. The analysis of the dependability of such systems is a particularly complex task that mandates modeling capabilities in both the discrete and in the continuous domains. To tackle this problem a multi-level approach is presented here, which is based on abstract functional models to capture the behavior of the whole system, and on detailed structural models to cope wi ...

Keywords: CAN bus, automotive, fault injection

#### 15 IP switching—ATM under IP

Peter Newman, Greg Minshall, Thomas L. Lyon

April 1998 IEEE/ACM Transactions on Networking (TON), Volume 6 Issue 2

Full text available: pdf(154.32 KB) Additional Information: full citation, references, citings, index terms

**Keywords**: Internet protocol, asynchronous transfer mode, broadband communication, communication system control, data communication, packet switching, protocols

#### 16 AMRoute: ad hoc multicast routing protocol

Jason Xie, Rajesh R. Talpade, Anthony Mcauley, Mingyan Liu December 2002 **Mobile Networks and Applications**, Volume 7 Issue 6

Full text available: pdf(216.21 KB)

Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index</u> <u>terms</u>

The Ad hoc Multicast Routing protocol (AMRoute) presents a novel approach for robust IP Multicast in mobile ad hoc networks by exploiting user-multicast trees and dynamic logical cores. It creates a bidirectional, shared tree for data distribution using only group senders and receivers as tree nodes. Unicast tunnels are used as tree links to connect neighbors on the *user-multicast tree*. Thus, AMRoute does not need to be supported by network nodes that are not interested/capable of multica ...

Keywords: IP multicast, mobile ad hoc networks, network protocols, routing

## 17 Wireless home networks: Design and implementation of the HiperLan/2 protocol

E. P. Vasilakopoulou, G. E. Karastergios, G. D. Papadopoulos

April 2003 ACM SIGMOBILE Mobile Computing and Communications Review, Volume 7 Issue 2

Full text available: pdf(1.50 MB) Additional Information: full citation, abstract, references

In recent years, wireless communication systems have experienced an enormous development, leading to the emergence of various wireless networks standards. These standards are characterized by different properties, such as their coverage, data rates, mobility and QoS support. Among them the HiperLan/2 standard is distinguished of its performance, supporting the provision of high-speed integrated services. Its centralized Medium Access Control protocol though is the most critical and complex funct ...

<sup>18</sup> Routers with a single stage of buffering



Sundar Iyer, Rui Zhang, Nick McKeown

August 2002 ACM SIGCOMM Computer Communication Review, Proceedings of the 2002 conference on Applications, technologies, architectures, and protocols for computer communications, Volume 32 Issue 4

Full text available: pdf(253.61 KB) Additional Information: full citation, abstract, references, index terms

Most high performance routers today use combined input and output queueing (CIOQ). The CIOQ router is also frequently used as an abstract model for routers: at one extreme is input queueing, at the other extreme is output queueing, and in-between there is a continuum of performance as the speedup is increased from 1 to N (where N is the number of linecards). The model includes architectures in which a switch fabric is sandwiched between two stages of buffering. There is a rich and ...

**Keywords**: buffers, constraint sets, routers, switching

19 A pipelined, multiprocessor architecture for a connectionless server for broadband ISDN

Daniel S. Omundsen, A. Roger Kaye, Samy A. Mahmoud April 1994 IEEE/ACM Transactions on Networking (TON), Volume 2 Issue 2

Full text available: pdf(1.21 MB) Additional Information: full citation, references, citings, index terms

20 Xunet 2: lessons from an early wide-area ATM testbed

Charles R. Kalmanek, Srinivasan Keshav, William T. Marshall, Samuel P. Morgan, Robert C.

February 1997 IEEE/ACM Transactions on Networking (TON), Volume 5 Issue 1

Full text available: pdf(231.69 KB) Additional Information: full citation, references, index terms

Keywords: asynchronous transfer mode, available bit rate, constant bit rate, variable bit rate

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